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PROGRAMMABLE PULSE GENERATOR. OPERATING INSTRUCTIONS.(U)  
JAN 82 J W PARADISE, W B ALLEN

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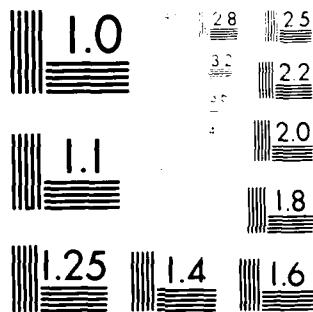
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Technical Document 459

## PROGRAMMABLE PULSE GENERATOR Operating Instructions

JW Paradise  
WB Allen

14 January 1982

Covers work from January through March 1981

Prepared for  
Naval Sea Systems Command

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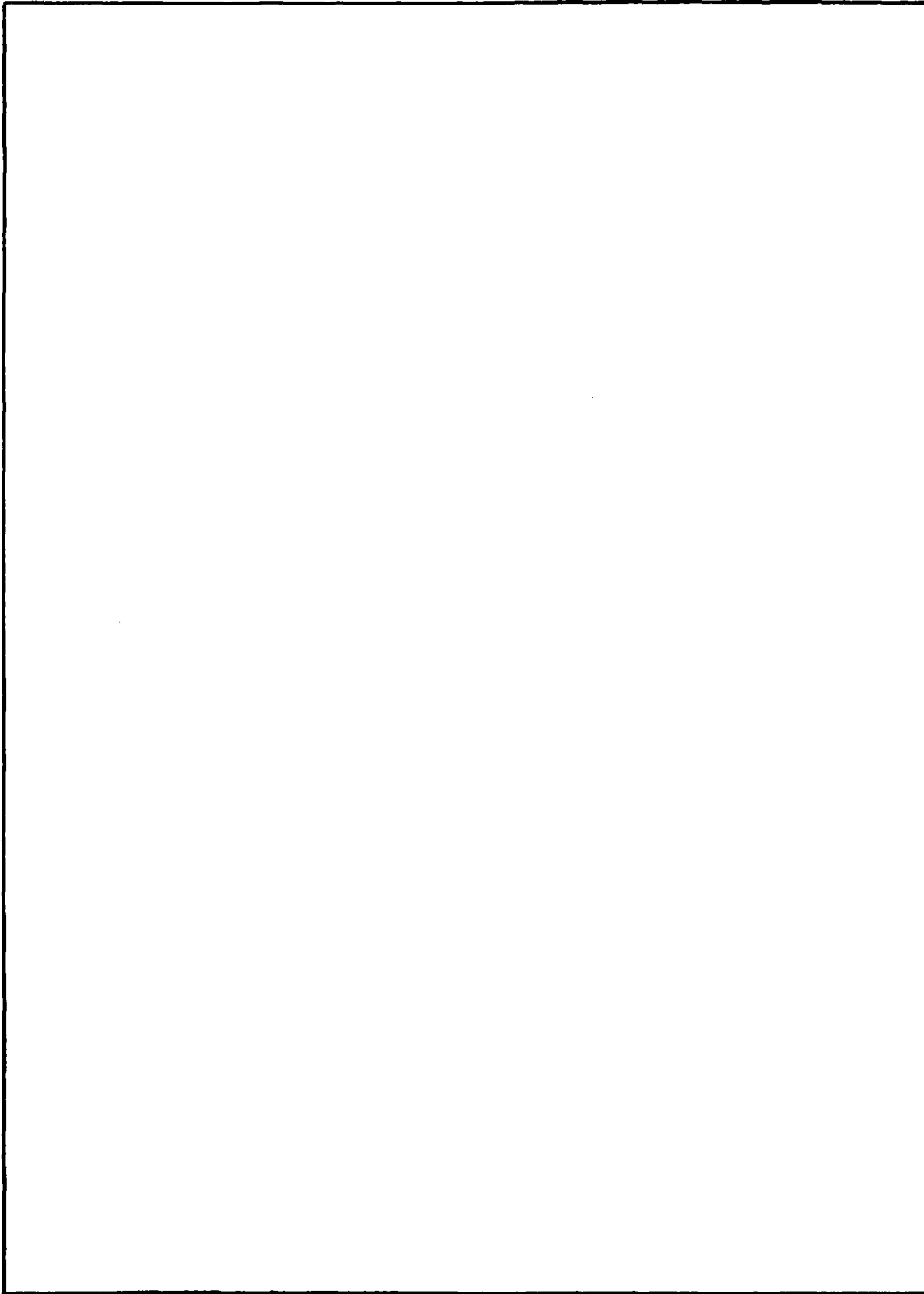
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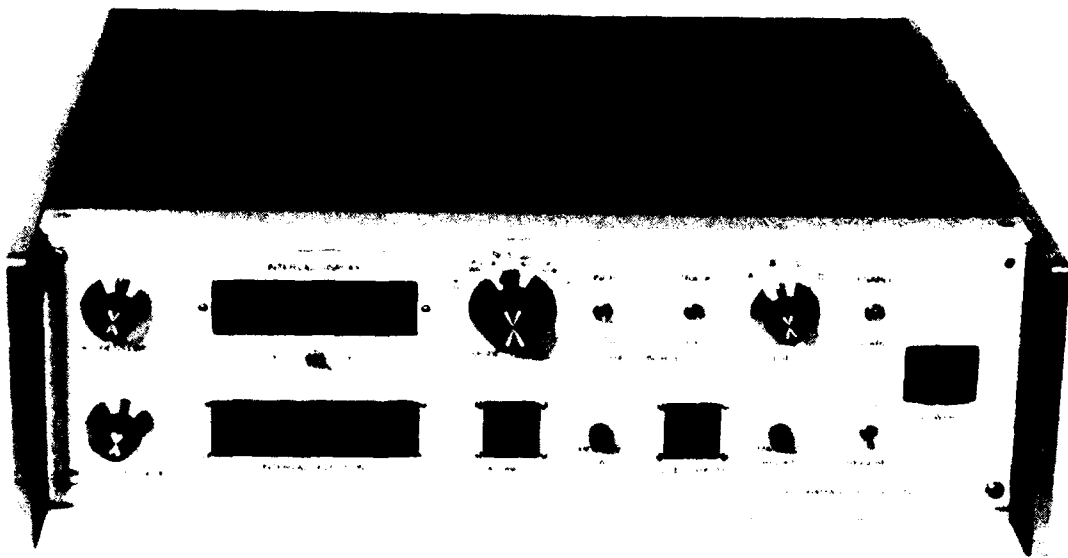
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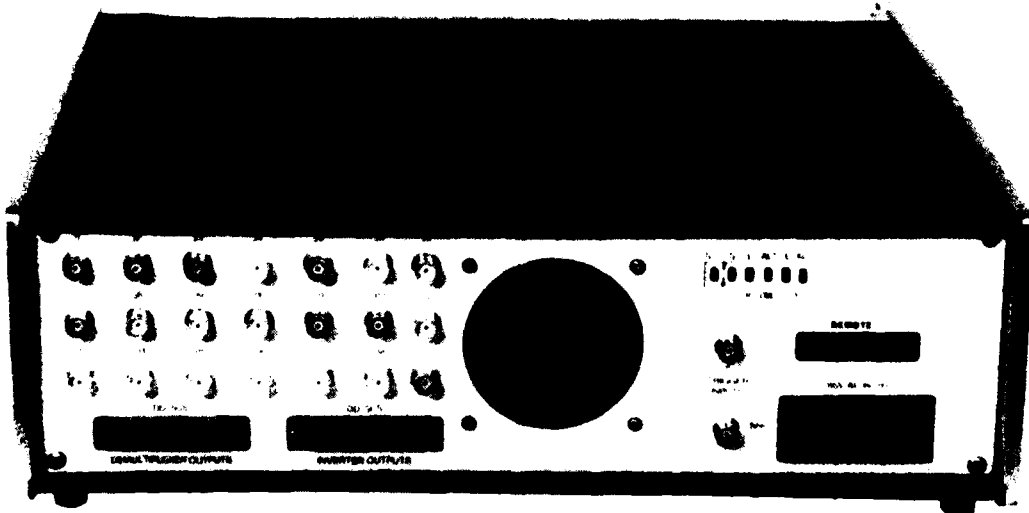
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FRONT VIEW



REAR VIEW



## INTRODUCTION

The Programmable Pulse Generator (facing page) is designed to be a versatile source of short bursts of 0.8- $\mu$ s trigger pulses and variable-width pulses whose spacings and widths can be programmed over a wide range. It can be used as a source of precision complex logic signals with square or rectangular waveforms and as a source of control signals for sequential operations.

In its basic form, the generator can produce a sequence of from 1 to 16 0.8- $\mu$ s trigger pulses at intervals that can be preselected over a range of 1 to 999.999. These pulses toggle an interval flip-flop to produce a sequence of eight pulses with preselected widths and spacings. Internal circuitry demultiplexes the 16 serial 0.8- $\mu$ s pulses and the 8 variable-width pulses onto 24 parallel output lines. The number of pulses in these two sequences is controlled by selecting the upper and lower limits of the memory address counter. A prescaler produces minimum timing intervals of 1, 10, 100, and 1000  $\mu$ s, providing minimum time intervals of 1 ms and maximum time intervals of 999 s.

The versatility of the pulse generator has been improved by incorporating two control memory address multiplexers and control circuitry so that the generator can be operated on either memory while a new sequence of timing intervals is being written into the other memory. The dual memories make it possible to change pulse sequences with no interruption in operation. After both memories are loaded, the generator can be switched to the alternate mode, which generates a sequence controlled by memory 1 followed immediately by a sequence controlled by memory 2. The alternate mode can generate a sequence of up to 32 0.8- $\mu$ s pulses and up to 16 pulses of preselectable widths and spacings. These two sequences of 32 and 16 pulses are also demultiplexed onto 48 parallel output lines.

A shift mode is available. It permits the interval between one or more of the 0.8- $\mu$ s pulses in the sequence to be increased or decreased a preselected amount either on command or each time the sequence is repeated. This mode is useful in such applications as the range gating of moving target signals

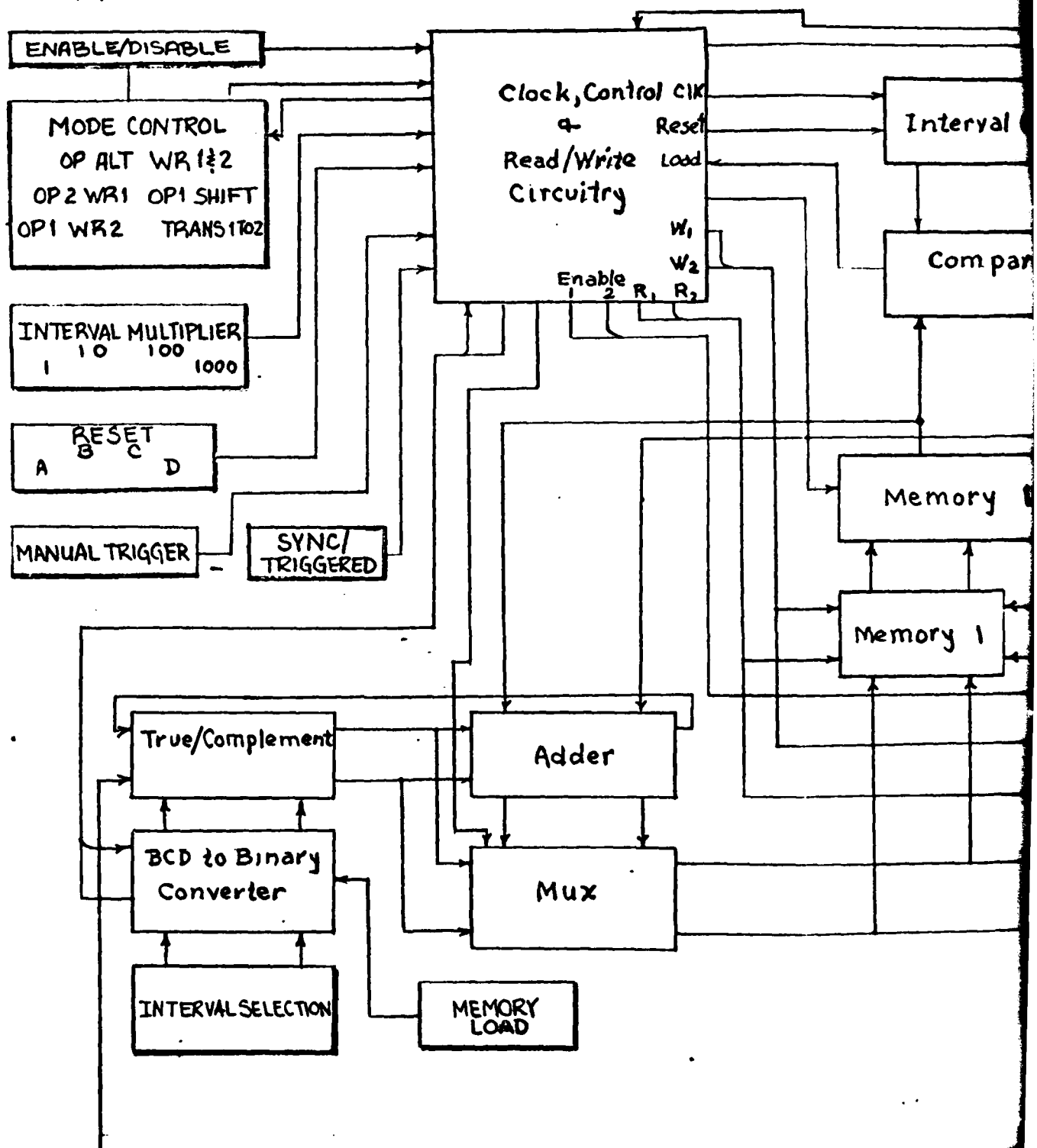
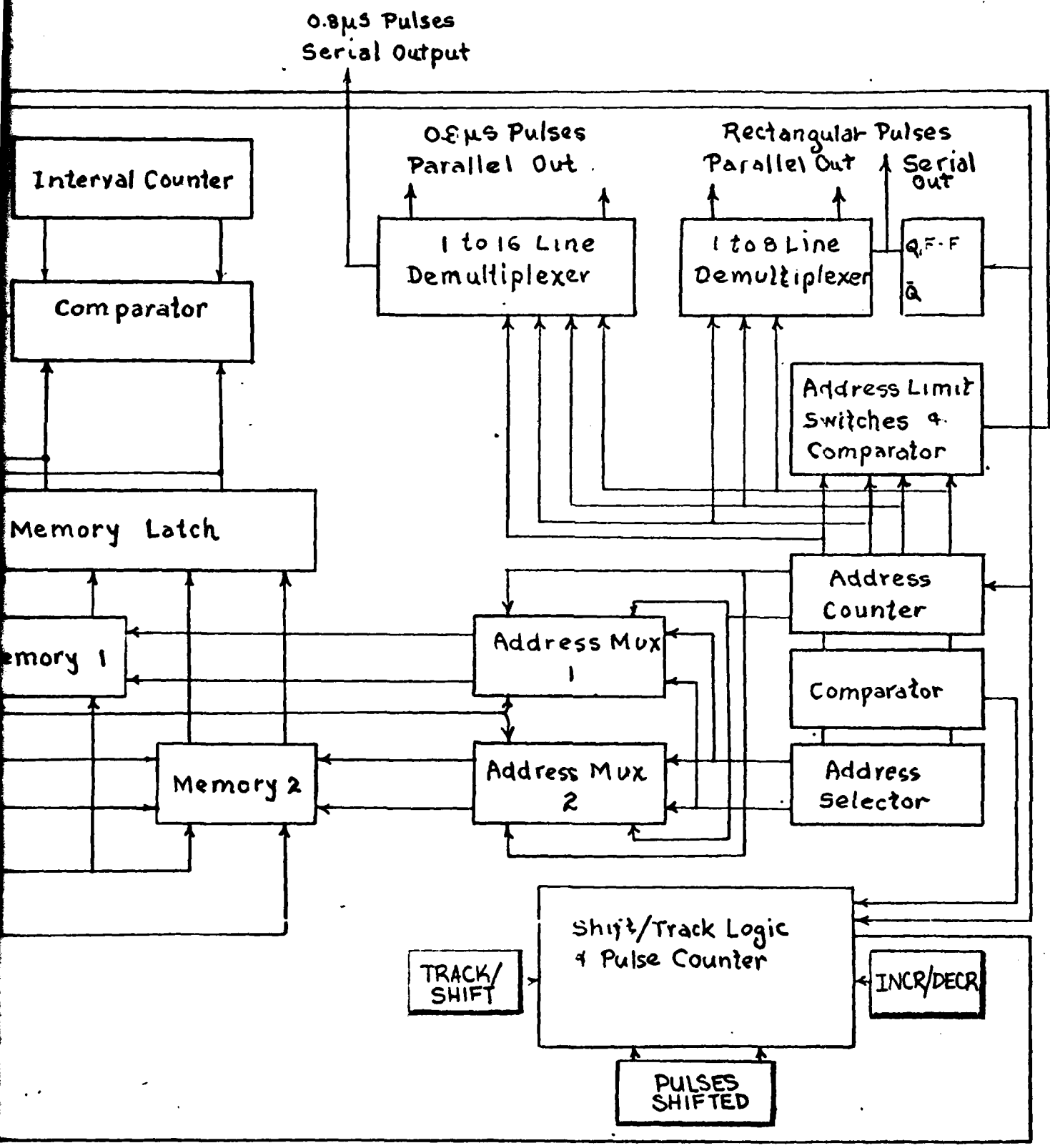


Figure 1. Block diagram.



and in control applications in which some control signals must shift slightly with respect to the initiate signal during each command sequence.

The generator can be operated as a free-running pulse generator to produce a repetitive waveform whose repetition interval is equal to the preselected sequence length. This repetitive waveform can be synchronized with an external trigger. As a triggered pulse generator, it produces one preselected sequence each time it receives an external trigger. In the alternate mode, it produces one double sequence - one sequence controlled by each memory - on every external trigger pulse.

#### PANEL CONTROLS AND FUNCTIONS

Figure 1 (facing page) is a functional block diagram of the pulse generator, and figure 2 (last page of document) is a sketch of the front and back panel layouts showing the locations of the various controls and interfaces. The upper and lower limits of the memory address counter are determined by the memory ADDRESS LIMIT control. This control selects LA+UA, LB+UB, or LA+UB, where LA and LB are two lower limits and UA and UB are two upper limits for the address counters. These four limits are determined by two 8-pole DIP switches located on the electronic component assembly, which are normally set at LA = 0, LB = 8, UA = 7, and UB = 15. These settings give memory address ranges of 0-7, 8-15, and 0-15, to provide for generating either two different 8-pulse sequences or one 16-pulse sequence. By writing two different 8-word programs into the 0-7 and 8-15 halves of memory 1, either of two 8-pulse sequences can be selected without causing any downtime during the change. When memory 1 and memory 2 are each programmed with two different 8-word programs, the generator can produce up to four different 8-pulse sequences, which can be selected without interrupting the operation.

The main clock interval selector or INTERVAL MULTIPLIER determines the frequency of the interval counter clock and hence the increments in time of the INTERVAL SELECTION switch. The output of the 10-MHz clock oscillator is divided by 10 to provide 10 equally spaced control and timing pulses and a 1-MHz output to the clock decade dividers. The three decade dividers and multiplexer provide timing interval increments of 1, 10, 100, and 1000  $\mu$ s.

The INTERVAL SELECTION switch, a six-decade BCD-coded thumbwheel switch, in conjunction with the INTERVAL MULTIPLIER switch, determines the spacings between the 0.8- $\mu$ s pulses in the output sequence. Pulse spacings between 1  $\mu$ s and 1 s, 10  $\mu$ s and 10 s, 100  $\mu$ s and 100 s, or 1 ms and 999.999 s can be obtained. In the shift mode (the three clockwise positions of the MODE CONTROL), the INTERVAL SELECTION switch is used to determine the increment by which the selected pulses are shifted each time the INCR/DECR switch is activated.

The MEMORY LOAD switch (the start convert and write function) is a momentary pushbutton switch that starts converting to a binary number the BCD number which is set into the INTERVAL SELECTION switch. In those modes that load the memory (the three counterclockwise positions of the MODE CONTROL), a pulse generated by the BCD-to-binary converter initiates a memory write pulse when the conversion is completed.

The ADDRESS selector, a hexadecimal-coded thumbwheel switch, is used to select the memory addresses during programming of the generator. In the shift mode it determines at which pulse in the sequence the shifting is to start. It is also used to determine the pulse interval that is to be measured and displayed.

The MODE CONTROL causes the generator to perform one of six functions, in the following switch positions, reading clockwise. The first three positions constitute the normal operating mode; the last three, the shift mode.

OP 1 WR 2 - Operate on memory 1 and write in memory 2

OP 2 WR 1 - Operate on memory 2 and write in memory 1

OP ALT - Operate on memories 1 and 2 on alternate pulse sequences

WR 1&2 - Write simultaneously in both memories

OP 1 SHIFT - Operate in the shift mode

TRANS 1 to 2 - Transfer data from memory 1 to memory 2.

## MODAL FUNCTIONS

The pulse generator is usually operated in the OP 1 WR 2 or OP 2 WR 1 position of the MODE CONTROL. In OP 1 WR 2 the generator can produce a sequence of pulses controlled by the program stored in memory 1 while a new program is being written into memory 2. In OP 2 WR 1 the generator can produce a sequence of pulses controlled by the program in memory 2 while a new program is being written into memory 1. In the OP ALT position, the generator can produce a 32-pulse sequence by producing the 16-pulse sequence controlled by memory 1 followed immediately by the 16-pulse sequence controlled by memory 2. With the SYNC/TRIGGERED switch on SYNC, the double sequence will be repeated until some of the controls are changed. An external trigger will synchronize the pulse sequence. When that switch is on TRIGGERED, the generator will produce one double output sequence each time an external trigger is received.

The three shift-mode positions of the MODE CONTROL were incorporated in the generator to permit increasing or decreasing (by preselected amounts) the time intervals between selected pulses in the output sequence while the generator is operating. Position WR 1&2 permits the same program to be written simultaneously into both memory 1 and memory 2. Position OP 1 SHIFT permits a set of contiguous pulses in the output sequence to be shifted a preselected amount on one or more pulse sequences. This operation is obtained by adding or subtracting the increment set into the INTERVAL SELECTION switch to or from the contents of the preselected addresses of memory 1. Position TRANS 1 to 2 is used to transfer the program from memory 1 to memory 2 after the original program in memory 2 has been modified by operating the generator in the OP 1 SHIFT position.

The INCR/DECR, TRACK/SHIFT, and PULSES SHIFTED controls are used only in the shift mode. The INCR/DECR control is a momentary on-off-on switch. When flipped to INCR, it causes the number set into the INTERVAL SELECTION switch to be added to the number in the memory cells at the locations specified by the ADDRESS selector and the PULSES SHIFTED control. Similarly when the switch is flipped to DECR, the number set into the INTERVAL SELECTION switch is subtracted from the number read from the specified memory cells. The

memory ADDRESS switch selects the first pulse spacing to be modified, and the PULSES SHIFTED switch determines the total number of pulse spacings that will be altered. The E/O on-off-on toggle switch on the back panel (fig 2) can inhibit the shifting of the odd or even pulses. With the TRACK/SHIFT switch in the SHIFT position, the selected pulses will be shifted the specified amount once each time the INCR/DECR switch is activated. With the TRACK/SHIFT switch in the TRACK position, activating the INCR/DECR switch will cause the selected pulses to be shifted the specified amount during each output pulse sequence - until the TRACK/SHIFT switch is returned to SHIFT.

In position A of the RESET control, the interval counter will be reset each time its content equals the number in the memory output buffer. The same thing occurs in position B, but only on the even matches; in position C, but only on the odd matches; and in position D, but only at the end of the complete output sequence. Each type of reset has its advantages and disadvantages depending on the total duration of the pulse sequence to be generated, how the pulse sequence is defined, and the mode of operation. An output pulse sequence in which all the pulses are specified with reference to the input trigger pulse can be programmed more conveniently with RESET position D. For example a sequence of 0.8- $\mu$ s pulses at 10, 20, 40, 80, 160, 320, 640, and 1280  $\mu$ s can be programmed most conveniently by using RESET position D - in which the interval counter is reset after each complete output pulse sequence has been generated. Thus, the above set of intervals can be written directly into the memory as given. Also, the intervals between one or more of the 0.8- $\mu$ s output pulses can be changed, with the timing of all the other pulses in the sequence staying the same relative to the input trigger.

If (1) each pulse in the output sequence is specified by its time of occurrence relative to the preceding pulse, starting with the input trigger pulse, or (2) the duration of the total pulse sequence is greater than 999 999 times the shortest duration between any two 0.8- $\mu$ s pulses in the output sequence, then RESET position A should be used. With RESET A, the interval counter is reset each time its count matches the number in the memory buffer; therefore an eight-cycle burst of 10-kHz square waves can be generated by writing 50  $\mu$ s into each of the 16 memory addresses, which toggles a flip-flop with the output sequence of 0.8- $\mu$ s pulses. Longer duration output sequences

can be produced with RESET A because any count up to the full count of the interval counter (999 999) can be used between adjacent 0.8- $\mu$ s output pulses.

Some of the manual controls could disrupt the generator if they were changed at the wrong time. To avoid this difficulty, the switch outputs are fed to a control buffer register. The control registers are loaded at the end of each output pulse sequence or whenever the MANUAL TRIGGER is activated. The buffer register load pulse can be inhibited by throwing the ENABLE/DISABLE switch to DISABLE to prevent the contents of the control register from being changed. Thus the controls can be changed without affecting the generator until this switch is flipped back to ENABLE.

The MANUAL TRIGGER starts a new pulse sequence by resetting both the interval counter and the address counter and triggering a memory read cycle. It also transfers the control settings to the control buffer registers.

The SYNC/TRIGGERED switch selects free-running or triggered operation of the generator. Setting the switch to SYNC lets the generator free-run so that one output sequence follows immediately after another. Under these conditions the output pulse sequence can be synchronized with an external trigger pulse. Setting the switch to TRIGGERED inhibits the generator until it receives an external pulse. The generator will then produce an output pulse sequence each time it receives an external trigger pulse. Internal trigger inhibit circuitry is available that will inhibit the external trigger while the pulse sequence is being generated. The inhibit circuitry can also be set so that once the generator is triggered it cannot be retriggered for 1, 10, 100, or 1000  $\mu$ s. Two TRIGGER INPUT BNC receptacles (1 and 2) are provided on the back panel. The  $T_1$  and  $T_2$  switches, also on the back panel, enable the trigger inputs for positive-going or negative-going logic level pulses.

#### OPERATION IN NORMAL OPERATING MODE

The easiest way to explain how to operate the generator is to describe the programming of several simple pulse sequences. Consider programming the generator to produce a sequence of 0.8- $\mu$ s pulses at 100, 200, 300, 400, 500, ... 1600  $\mu$ s at the trigger outputs and a 5-kHz square wave at the  $Q_1$



output of the address counter. After the POWER switch has been turned on, the lower and upper limits on the address counter are set by turning the ADDRESS LIMIT switch to 0-15. The INTERVAL MULTIPLIER is set at 1 and the MODE CONTROL is set to OP 2 WR 1 (operate on memory 2, write in memory 1). The counter RESET is set to D and the SYNC/TRIGGERED switch is set to SYNC. The control ENABLE/DISABLE switch is set to ENABLE and the MANUAL TRIGGER is pressed to load the switch settings into the control buffer. The generator is now ready to be programmed. The INTERVAL SELECTION control is set to 100 and the ADDRESS control is set to 0, then the MEMORY LOAD switch is pressed. The INTERVAL SELECTION switch is advanced to 200 and the ADDRESS switch is advanced to 1, then the MEMORY LOAD switch is pressed. This procedure is continued, advancing the INTERVAL SELECTION switch by 100 each time, until it is set to 1600 and the ADDRESS switch is set to 15, which completes the programming of memory 1. The MODE CONTROL switch is then changed to OP 1 WR 2 (operate on memory 1 and program memory 2). If the generator doesn't produce an output, press MANUAL TRIGGER. The waveform at the trigger output should be as shown in figure 3A and the waveform at the  $Q_1$  output of the address counter should be as shown in figure 4A.

While the generator is operating in OP 1 WR 2 on this program, it would be interesting to see what the generator outputs are for each RESET setting and each ADDRESS LIMIT setting. Switch the RESET control to A. The waveforms at the trigger and address counter  $Q_1$  outputs should be as shown in figures 3B and 4B, respectively. The corresponding outputs for RESET settings B and C are shown in figures 3C, 3D, 4C, and 4D. Study each of the waveforms to determine how they are produced from the program.

Return the RESET switch to A and change the ADDRESS LIMIT switch to 0-7. The generator should now produce the waveforms shown in figures 5A and 6A, which are the same as the first halves of figures 3B and 4B, respectively. Now change the ADDRESS LIMIT switch to 8-15. The generator should now produce the waveforms shown in figures 5B and 6B, which are the same as the last halves of figures 3B and 4B, respectively. By writing two different 8-word programs into the 0-7 and 8-15 halves of memory 1, either of two 8-pulse sequences can be selected without downtime.

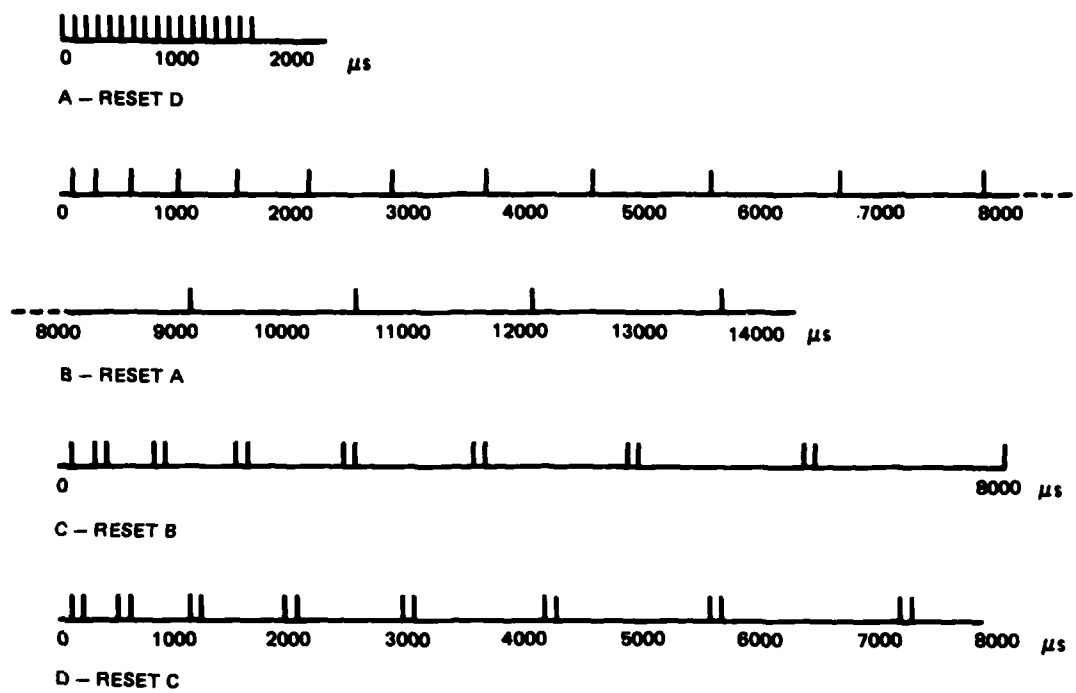


Figure 3. 0.5- $\mu s$  pulse output sequence.

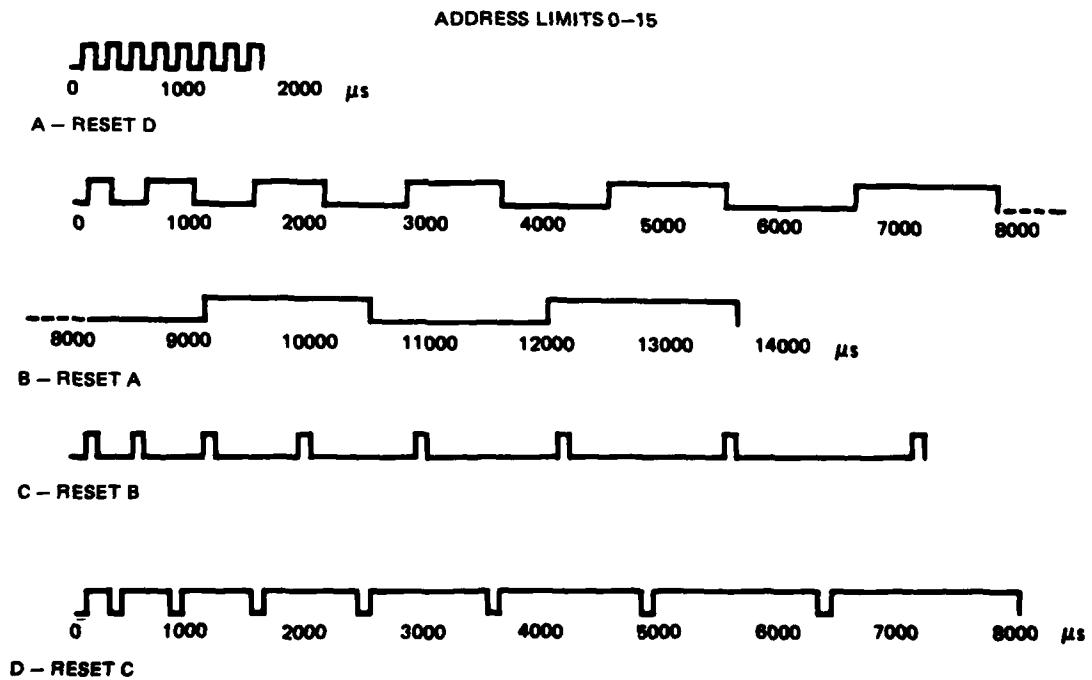


Figure 4.  $Q_1$  output of address counter.

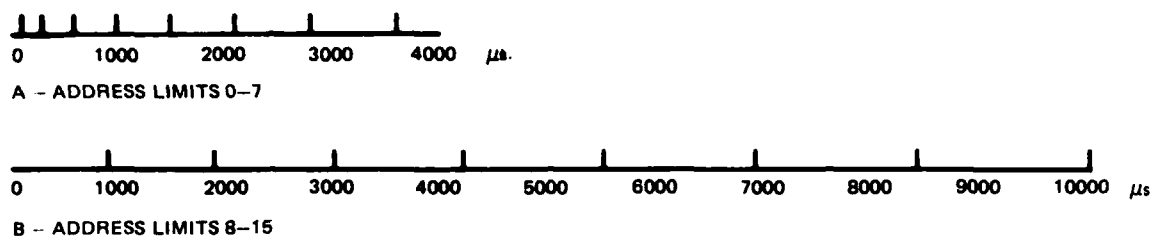


Figure 5. 0.5- $\mu$ s pulse sequence output.

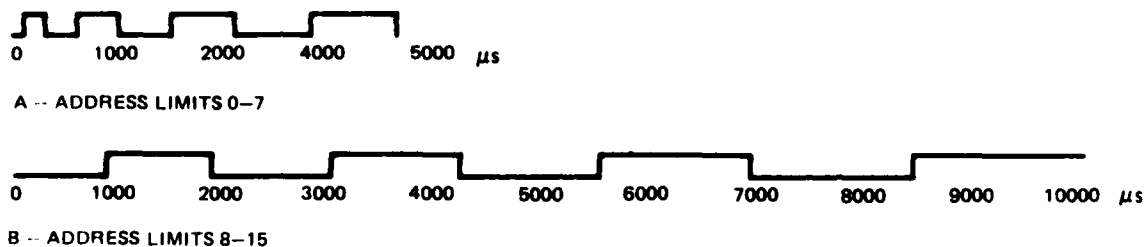


Figure 6.  $Q_1$  output of address counter.

To check the operation of the INTERVAL MULTIPLIER control, change the RESET control to D and the ADDRESS LIMIT switch to 0-15; then sequence the INTERVAL MULTIPLIER control through all its positions, stopping at each position to check the waveforms at the  $Q_1$  output of the address counter. The 5-kHz square wave should change to 500, 50, and 5-Hz, respectively as the INTERVAL MULTIPLIER is stepped through the  $10^1$ ,  $10^2$ , and  $10^3$  positions.

While the generator is operating on the program in memory 1, a program can be written into memory 2 that will produce a 0.8- $\mu$ s output pulse every 100  $\mu$ s at the trigger output or a 5000-Hz square wave at the  $Q_1$  output of the address counter when the generator is operated on memory 2 with counter RESET at A. This can be achieved by setting the INTERVAL SELECTION switch to 100 and the ADDRESS selector switch to 0, then pressing the MEMORY LOAD switch. The INTERVAL SELECTION switch is left at 100 while the ADDRESS selector is sequenced through all 16 addresses, and the MEMORY LOAD switch is pressed after each change of the ADDRESS selector. After the memory is loaded, change the MODE CONTROL switch to OP 2 WR 1 (operate on memory 2, program memory 1). If the generator doesn't produce an output, press MANUAL TRIGGER. The outputs should be as shown in figures 3A and 4A, which are the same as the waveforms produced when the generator is operating on memory 1 with position D on the counter RESET. With this program the generator will not operate or will produce only a very short sequence when the RESET control is changed to B, C, or

D, because once the interval counter reaches 100, the number in the second memory address is also 100 and the generator hangs up.

Return the RESET control to position A and change the MODE CONTROL to OP ALT (operate on both memory 1 and memory 2). In OP ALT the generator can be operated in either of two different ways by means of the ALT/DBL switch on the rear panel. With this switch in the ALT position, the generator will produce an output pulse sequence controlled by the program in memory 1 when TRIGGER INPUT 1 is activated, or an output pulse sequence controlled by the program in memory 2 when TRIGGER INPUT 2 is activated. With the switch in the DBL position, the generator will produce a pulse sequence controlled by memory 1 followed immediately by a pulse sequence controlled by memory 2 when TRIGGER INPUT 1 is activated, or a pulse sequence controlled by memory 2 followed immediately by a pulse sequence controlled by memory 1 when TRIGGER INPUT 2 is activated. The waveforms at the trigger output and the  $Q_1$  output of the address counter, with the switch in the DBL position and TRIGGER INPUT 1 activated, should be as shown in figures 7 and 8.

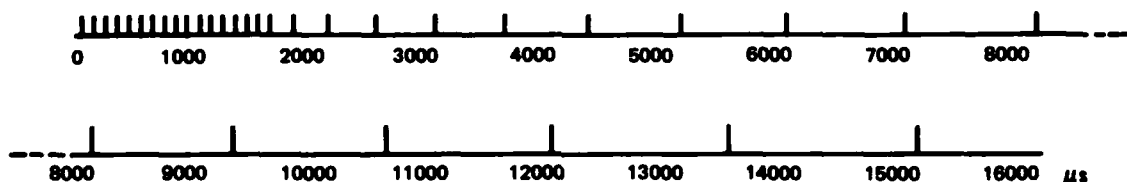


Figure 7. 0.5- $\mu$ s pulse output sequence, alternate mode.

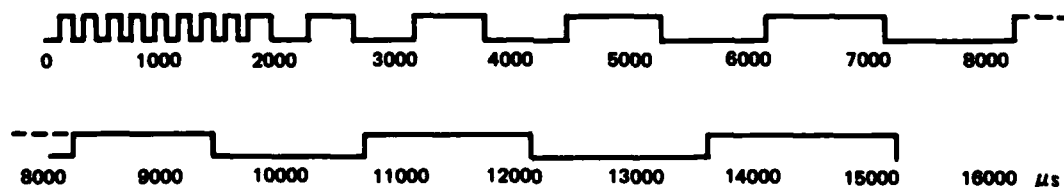


Figure 8.  $Q_1$  output of address counter, alternate mode.

#### OPERATION IN SHIFT MODE

The three clockwise positions of the MODE CONTROL are used when it is desired to change the spacings between one or more of the 0.8- $\mu$ s pulses in the output sequence by a predetermined amount while the generator is operating.

As an example, consider that the generator is programmed to produce sixteen 0.8- $\mu$ s pulses at 500- $\mu$ s intervals and that the spacing between pulses 4 and 5 is to be increased 50  $\mu$ s on command. To make the pulse numbers in the following discussion match the address control setting, the 16 output pulses are numbered 0-15. The generator is prepared for operation in OP 1 SHIFT by first setting the RESET control to A, the ADDRESS LIMIT control to 0-15, and the MODE CONTROL to WR 1&2 (write simultaneously in memory 1 and memory 2).

The programming of both memories proceeds as in the normal operating mode, OP 1 WR 2 or OP 2 WR 1. The INTERVAL SELECTION switch is set to 500 and the ADDRESS selector is set to 0, then the MEMORY LOAD switch is pressed. The INTERVAL SELECTION switch is left at 500 while the ADDRESS selector is stepped through all 16 positions, the MEMORY LOAD switch being pressed after each change of the ADDRESS switch. After the memories are loaded, the MODE CONTROL is switched to OP 1 SHIFT.

To obtain the change in interval spacing between pulses 4 and 5 on command, the TRACK/SHIFT switch is flipped to SHIFT, the ADDRESS selector is set to 5, and the PULSES SHIFTED control is set to 1. The INTERVAL SELECTION switch is set to 50  $\mu$ s, and the MEMORY LOAD switch is pressed to convert the BCD number 50 to a binary number and store it in the converter output buffer. If the generator is not producing an output, press MANUAL TRIGGER to start the generator. Now each time the INCR/DECR switch is flipped to the INCR position, the interval between the 4th and 5th pulses is increased by 50  $\mu$ s on the next output sequence. Each time the INCR/DECR switch is flipped to the DECR position, the spacing between the 4th and 5th pulses is decreased by 50  $\mu$ s on the next output sequence.

To obtain a 50- $\mu$ s change in the spacing between pulses 4 and 5 on every pulse sequence, the TRACK/SHIFT switch is set to TRACK. Now when the INCR/DECR switch is flipped to INCR, the spacing between pulses 4 and 5 will be increased by 50  $\mu$ s during each pulse sequence until the TRACK/SHIFT control switch is set to SHIFT. Alternatively, the spacing between pulses 4 and 5 is decreased 50  $\mu$ s during each output sequence when the INCR/DECR switch is flipped to DECR. The magnitude of the change in pulse spacing can be altered by dialing the desired change into the INTERVAL SELECTION switch and pressing the

MEMORY LOAD switch. If the generator is operating in the TRACK phase of the shift mode, the change in pulse spacing will be altered on the next output sequence. If the generator is in the SHIFT phase of the shift mode, the change in pulse spacing will be altered the next time the INCR/DECR switch is flipped.

To change the spacings between a contiguous group of 0.5- $\mu$ s output pulses, the ADDRESS selector is set to the first interval that is to be altered and the PULSES SHIFTED control is set to the number of intervals that are to be changed. For example, if the intervals between pulses 4 to 9 are each to be changed by 10  $\mu$ s, the ADDRESS and PULSES SHIFTED controls are both set to 5. The INTERVAL SELECTION control is set to 10 and the MEMORY LOAD switch is pressed. The TRACK/SHIFT switch is set to SHIFT and the INCR/DECR switch is set to the desired position to activate the pulse shifting circuitry. A toggle switch on the electronic component assembly can be positioned so that the spacing of only the odd, only the even, or all pulses is changed.

With the RESET control on A, only the spacing between the selected output pulses will be changed and all the other pulse spacings will remain unchanged. This is not true at the other RESET positions. For example, when the generator is operating with RESET on D and the spacing between pulses 4 and 5 is increased, the spacing between pulses 5 and 6 will be decreased by an equal amount if the PULSES SHIFTED control is set to 1. With the RESET switch on D, a change in the spacing between only pulses 4 and 5 is achieved by setting the ADDRESS selector to 5 and the PULSES SHIFTED to 11 (15 - 4). That is, the program words must be modified for all pulses subsequent to the pulse spacing it is desired to change.

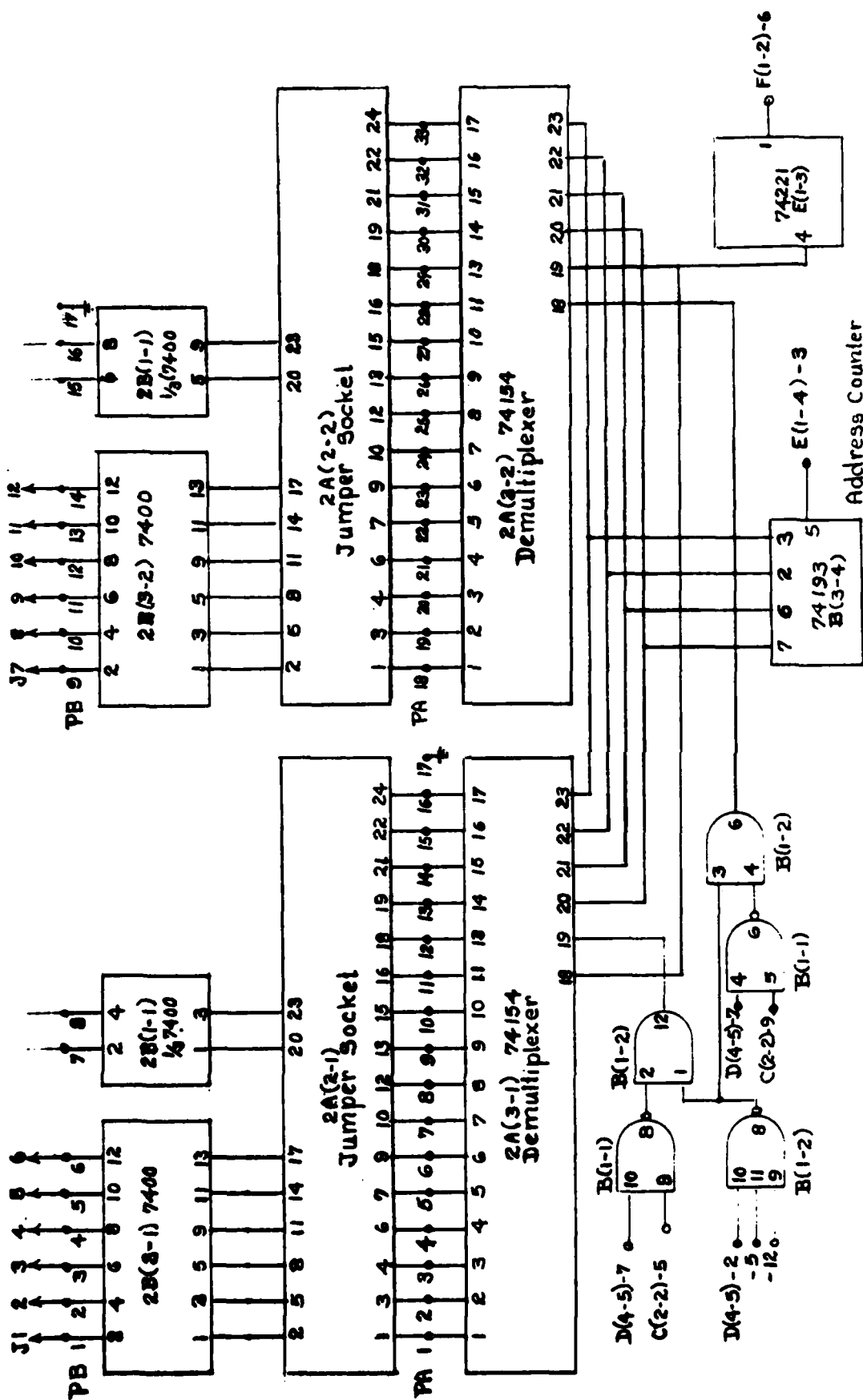
For the example illustrated, with RESET C (figure 3), the interval between pulses 4 and 5 can be changed by modifying the program word at address 5, because the interval counter is reset after pulse 5. For reset B and the same example, to change the spacing between only pulses 4 and 5 requires that the program words at addresses 5 and 6 be modified, because the interval counter is not reset until after pulse 6.

## OUTPUTS AND SIGNAL DEMULTIPLEXING

As mentioned in the introduction, both serial output pulse sequences are demultiplexed onto parallel output lines. As shown in figures 9 and 10, the sequence of 0.5- $\mu$ s pulses is demultiplexed onto 32 lines that are connected to pins 1-16 and 18-33 of the PA plug (fig 2). With the MODE CONTROL on OP 1 WR 2, OP 2 WR 1, or OP 1 SHIFT, the two demultiplexers [2A(3-1) and 2A(3-2)] are operated in parallel so that the same signals are present on the outputs of the two demultiplexers; thus the same signals are available at pins 1-16 and 18-33, respectively. With the MODE CONTROL on OP ALT, demultiplexer 2A(3-1) decodes the pulse sequence generated by memory 1 and demultiplexer 2A(3-2) decodes the pulse sequence generated by memory 2, so that the 32 output pulses are available on pins 1-16 and 18-33 of plug PA.

The outputs of demultiplexers 2A(3-1) and 2A(3-2) are also connected to 16 pins on each of four 24-pin DIP sockets [2A(2-1), 2A(2-2), 2A(1-1), and 2A(1-2)]. The other eight pins on DIP sockets 2A(2-1) and 2A(2-2) are connected to the inputs of 16 inverters. The outputs of the 16 inverters are connected to pins 1-16 of plug PB, and the outputs of 12 inverters (the first six inverters of each group of eight) are connected to BNC connectors J1-J12 (fig 2). Component carriers or short jumper leads can be used to connect any 8 of the 16 demultiplexer lines to the 8 inverter pins on each 24-pin jumper socket. With the MODE CONTROL on OP 1 WR 2, OP 2 WR 1, or OP 1 SHIFT, any or all 16 of the sequential output pulses can be inverted and fed to pins 1-16 of plug PB, and up to 12 of the selected pulses can be fed to BNC connectors J1-J12. With the MODE CONTROL on OP ALT, any 16 selected pulses of the 32 pulses in the double sequence can be inverted and fed to pins 1-16 on plug PB. Twelve of the selected pulses can also be connected to BNC connectors J1-J12.

As shown in figure 10, eight pins on DIP sockets 2A(1-1) and 2A(1-2) are connected to two 8-pin OR gates. The outputs of the two OR gates are connected to pins 30 and 31 of the PB plug and the clock input of two toggle flip-flops. The Q and  $\bar{Q}$  outputs of the two flip-flops are connected to pins 26-29 of plug PB. The Q outputs of the two flip-flops are also connected to BNC connectors JX and JY. This makes it possible to reconstruct two different



**Figure 9. Output decoders for 0.5- $\mu$ s pulses.**



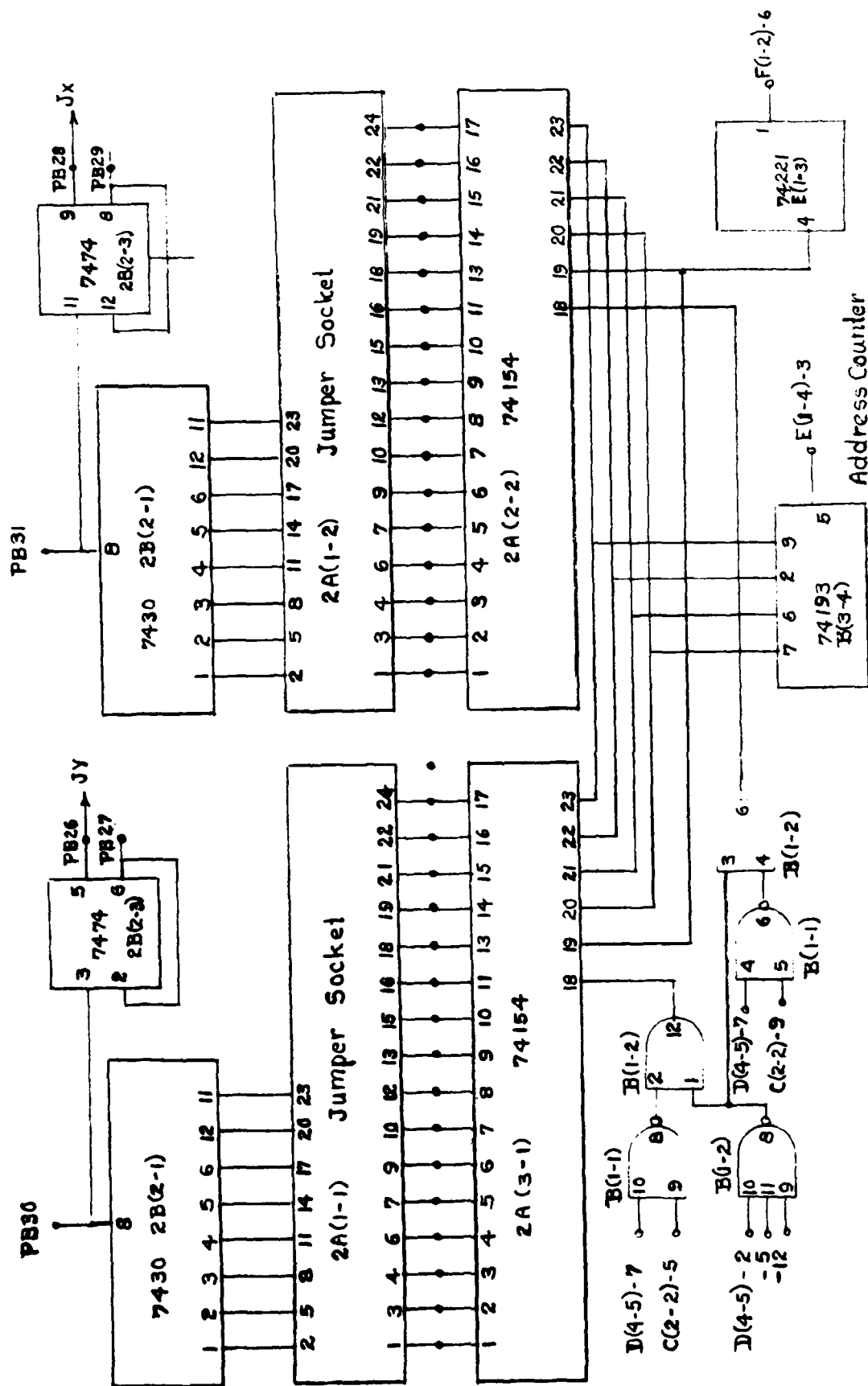


Figure 10. Reconstructed pulse sequence generators.

sequences of eight 0.5- $\mu$ s pulses each and two different four-pulse sequences with selectable pulse widths and spacings.

The positive-going pulses at the  $Q_1$  output of the address counter are demultiplexed by 2A(3-3) onto 8 lines for MODE CONTROL positions OP 1 WR 2, OP 2 WR 1, and OP 1 SHIFT or onto 16 lines for position OP ALT, as shown in figure 11. The outputs of the demultiplexer are connected to pins 34-49 of plug PA and 16 pins of a 24-pin DIP [2A(2-3)]. The other eight pins of the DIP are connected to the inputs of eight inverters, the outputs of which are connected to pins 18-24 of plug PB. The outputs of the first six inverters are also connected to BNC connectors J13-J18.

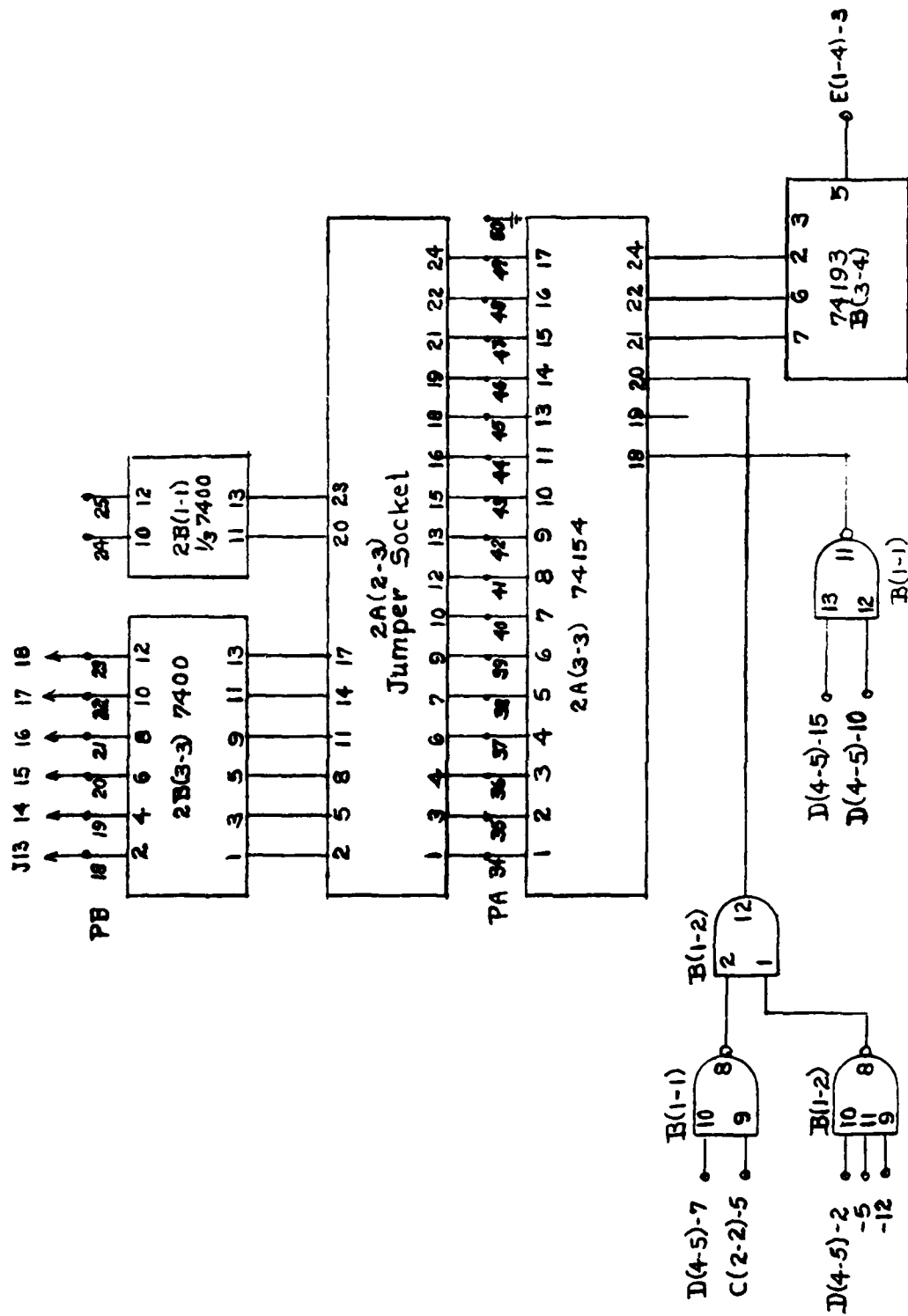
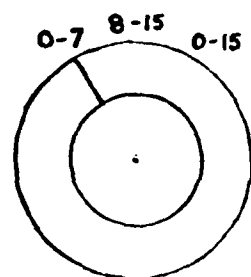
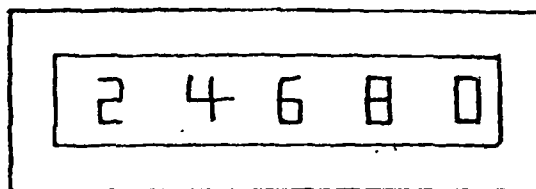


Figure 11. Output decoder for address counter  $Q_1$  output.

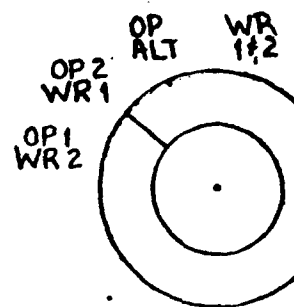


ADDRESS LIMIT

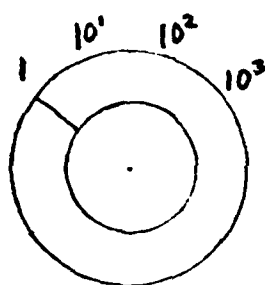
INTERVAL DISPLAY



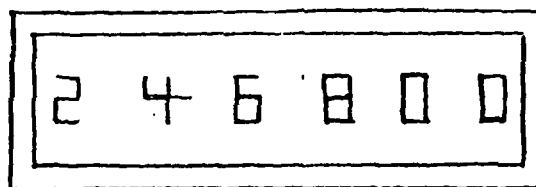
X1  $\rightarrow$  X.1



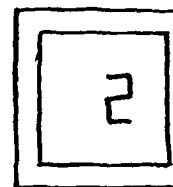
MODE CONT



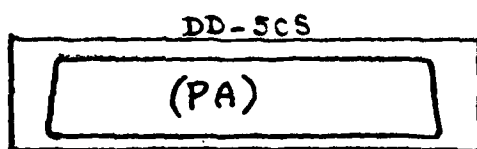
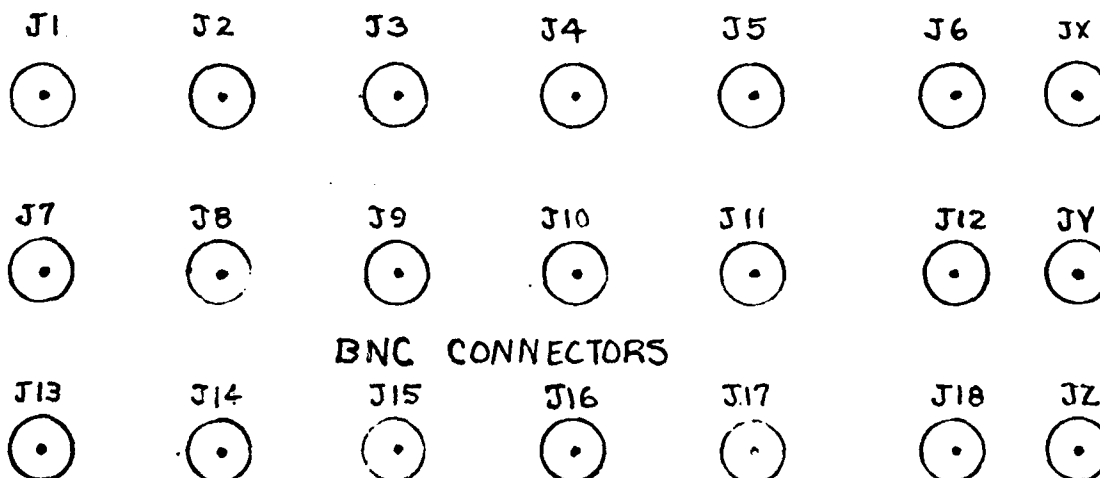
INTERVAL MULTIPLIER



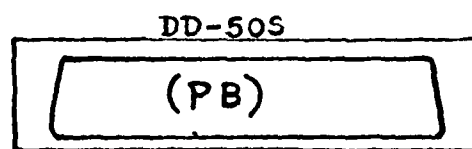
INTERVAL SELECTION



ADDRESS



DEMULTIPLEXER OUTPUTS



INVERTER OUTPUTS

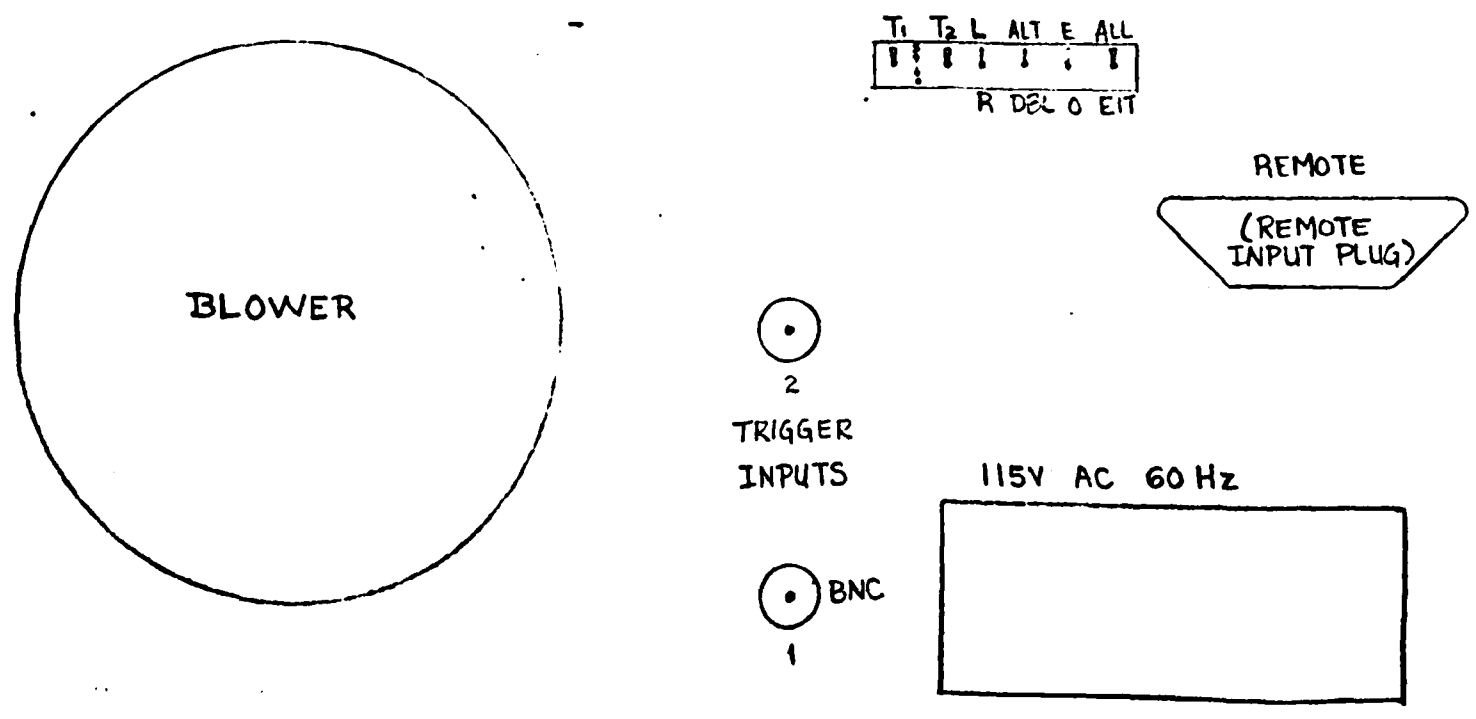
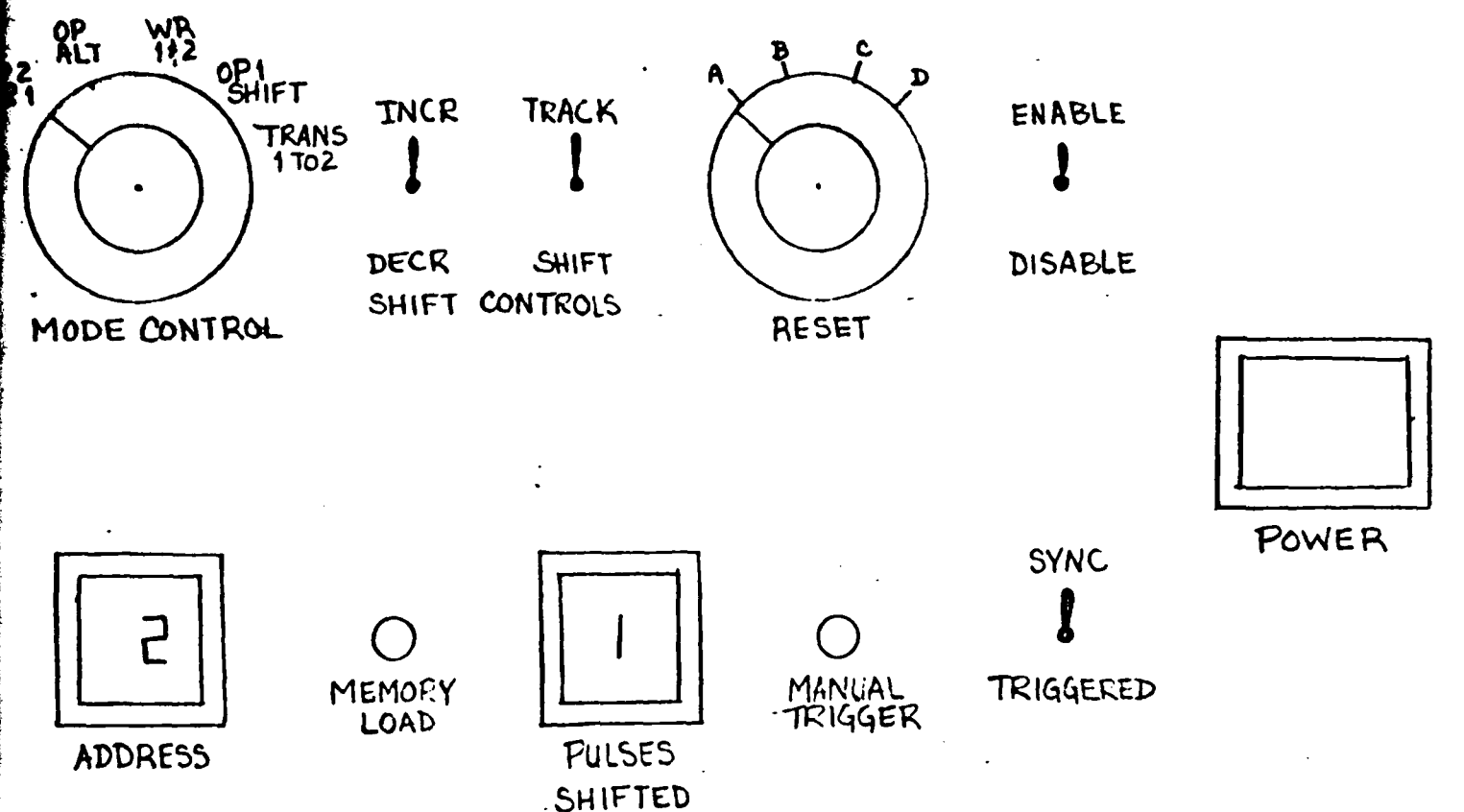


Figure 2. Front and rear panels.

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